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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,305	12/28/2001	Gee Sung Chae	2658-0283P	2901
2292	7590	10/05/2004	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			RUDE, TIMOTHY L	
			ART UNIT	PAPER NUMBER
			2883	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/028,305

Applicant(s)

SUNG CHAE ET AL.

Examiner

Timothy L Rude

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 July 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Ueda et al (Ueda) USPAT 6,078,365.

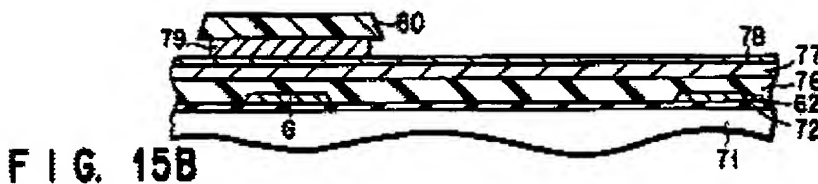
As to claim 1, Ueda discloses an embodiment in Figures 15A-15F (col. 12, line 58, through col. 18, line 33, especially col. 16, line 64, through col. 18, line 33) comprising: a substrate, 71; a gate electrode, G, over the substrate; a first semiconductor layer, 77, over the gate electrode; a second semiconductor layer, 78, over the first semiconductor layer and having a defined outer edge, source, S, and drain, D, electrodes (Applicant's first metal layer) on the second semiconductor layer, the first metal layer patterned in a same pattern as the second semiconductor layer such that the first metal layer and second semiconductor layer define the channel (Applicant's separation region). Please note that this is by way of only one photolithography pattern per Figures (Applicant's patterned in the same pattern).

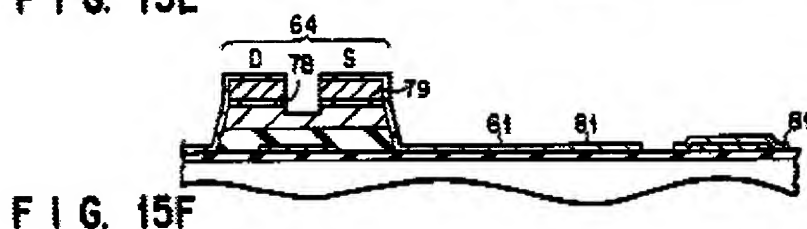
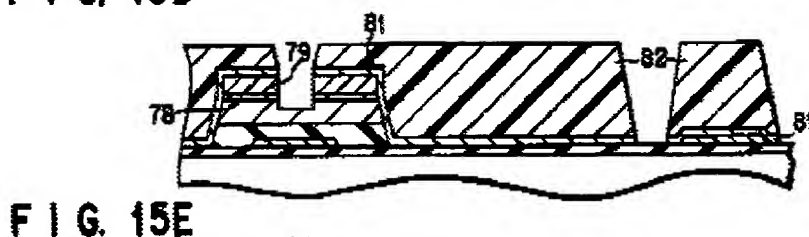
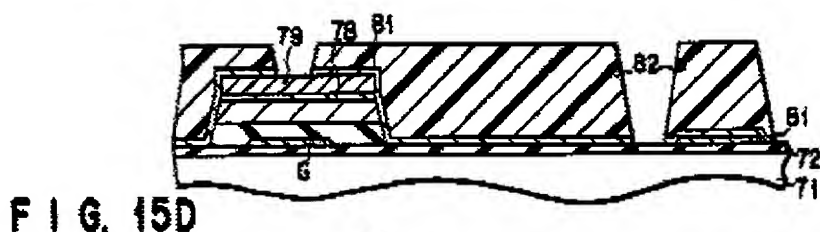
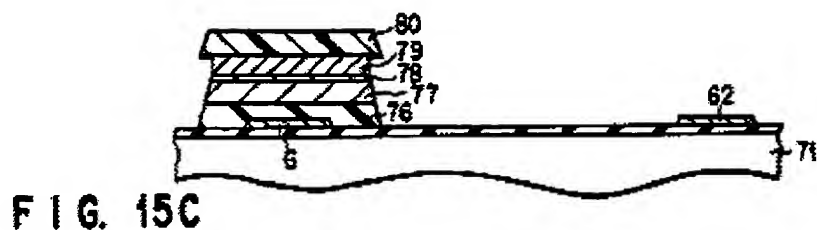
Ueda further discloses the use of source, S, and drain, D, comprised of Aluminum and Molybdenum disposed on Molybdenum (Mo/Al/Mo) (comprises

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Applicant's electrodes over the first metal layer), the source and drain electrodes patterned the same as the first metal layer and having a defined outer edge and the second semiconductor layer (col. 17, lines 22-42) define first upper portion of the separation region, and the source and drain electrodes include a second (Al) and a third (Mo) metal layer, in order to use a low resistance metal such as Aluminum for improved conductivity of the circuit components (col. 17, line 55, through col. 18, line 5).

The outer defined edges of the metal layers and silicon layers are all lined up and abut each other to define the channel as illustrated.





As to claim 8, Ueda discloses (col. 12, line 58, through col. 18, line 33, especially col. 16, line 64, through col. 18, line 33) the method of forming a liquid crystal display device, comprising: forming a gate electrode on a substrate; forming an active layer over the gate electrode; forming a first semiconductor layer over the active layer; forming a second semiconductor layer over the first semiconductor layer; forming a first metal layer over the second semiconductor layer patterning the first metal layer and the second semiconductor layer in a same pattern; and forming a source electrode and a drain electrode over the first metal layer.

The outer defined edges of the metal layers and silicon layers are all lined up and abut each other to define the channel as illustrated.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (APA) in view of Ueda et al (Ueda) USPAT 6,078,365.

As to claim 1, APA discloses a conventional liquid crystal display device in Figures 1-5 (Specification pages 1-5), comprising: a substrate, 1; a gate electrode, 3, over the substrate; a first semiconductor layer, 15, over the gate electrode; a second semiconductor layer, 17, over the first semiconductor layer, source, 5, and drain, 7, electrodes (Applicant's first metal layer) on the second semiconductor layer, the first metal layer patterned in a same pattern as the second semiconductor layer such that the first metal layer and second semiconductor layer define the channel, 30 (Applicant's separation region) per Figure 3C (specification page 3, lines 28-31). Please note that this is well known in the art to take only one photolithography pattern (Applicant's patterned in the same pattern).

APA does not explicitly disclose source and drain electrodes over the first metal layer, the source and drain electrodes patterned the same as the first metal layer and the second semiconductor layer define first upper portion of the separation region, and the source and drain electrodes include a second and a third metal layer.

Ueda teaches and embodiment in Figures 15A-15F (col. 12, line 58, through col. 18, line 33, especially col. 16, line 64, through col. 18, line 33) the use of source, S, and drain, D, comprised of Aluminum and Molybdenum disposed on Molybdenum (Mo/Al/Mo) (comprises Applicant's electrodes over the first metal layer), the source and drain electrodes patterned the same as the first metal layer and the second semiconductor layer (col. 17, lines 22-42) define first upper portion of the separation region, and the source and drain electrodes include a second (Al) and a third (Mo) metal

layer, in order to use a low resistance metal such as Aluminum for improved conductivity of the circuit components (col. 17, line 55, through col. 18, line 5).

Ueda is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to add source and drain electrodes over the first metal layer, the source and drain electrodes patterned the same as the first metal layer and the second semiconductor layer define first upper portion of the separation region, and the source and drain electrodes include a second and a third metal layer in order to use a low resistance metal such as Aluminum for improved conductivity of the circuit components.

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of APA with added source and drain electrodes over the first metal layer, the source and drain electrodes patterned the same as the first metal layer and the second semiconductor layer define first upper portion of the separation region, and the source and drain electrodes include a second and a third metal layer in order to use a low resistance metal such as Aluminum for improved conductivity of the circuit components.

As to claim 8, the method of forming a liquid crystal display device, comprising: forming a gate electrode on a substrate; forming an active layer over the gate electrode; forming a first semiconductor layer over the active layer; forming a second semiconductor layer over the first semiconductor layer; forming a first metal layer over the second semiconductor layer patterning the first metal layer and the second

semiconductor layer in a same pattern; and forming a source electrode and a drain electrode over the first metal layer, would have been obvious given the device structure above and the teachings of Ueda (col. 12, line 58, through col. 18, line 33, especially col. 16, line 64, through col. 18, line 33).

As to claim 2, APA discloses a device, further comprising: an insulating layer in between the gate electrode and the first semiconductor layer; a protective layer, 21, over the source and drain electrodes and defining a second upper portion of the separation region (Figure 3D) and a contact hole, 19b, exposing a portion of the drain electrode; and a pixel electrode, 23, in the contact hole (Figure 3E).

As to claim 3, APA in view of Ueda, as combined above, discloses the device of claim 1 above, wherein; the second metal layer includes aluminum (Al, Ueda, col. 17, lines 22-30).

As to claim 4, APA in view of Ueda, as combined above, discloses the device of claim 1 above, wherein the first and third metal layers are formed of the same material (Mo, Ueda, col. 17, lines 22-30).

As to claim 5, APA in view of Ueda, as combined above, discloses the device of claim 1 above.

The device of claim 1 above does not explicitly disclose a device wherein the first and third metal layers are formed of different materials.

Ueda teaches the use of a refractory metal of Cr or a Mo-Ta alloy (col. 12, lines 62-67) as art recognized equivalents suitable for the intended purpose of forming an undercoat conductive layer (MPEP 2144.07).

Ueda is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to use Cr or a Mo-Ta alloy for one of the first or third metal layers, resulting in the claimed device wherein the first and third metal layers are formed of different materials.

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of APA in view of Ueda with the Cr or a Mo-Ta alloy for one of the first or third metal layers, resulting in the claimed device wherein the first and third metal layers are formed of different materials.

As to claim 6, APA in view of Ueda, as combined above, discloses the device of claim 1 above, wherein the first and third metal layers include molybdenum (Mo, Ueda, col. 17, lines 22-30).

As to claim 7, APA in view of Ueda, as combined above, discloses the device of claim 4 above, wherein the first and third metal layers are formed include molybdenum (Mo, Ueda, col. 17, lines 22-30).

As to claim 9, the method of claim 8, wherein forming the source and drain electrodes includes forming a second metal layer over the first metal layer, forming a third metal layer over the first metal layer, and patterning the second and third metal layers in the same pattern as the first metal layer and second semiconductor layer in the channel region so that a channel portion of the first semiconductor layer is exposed, would have been obvious given the device structure above.

As to claim 10, APA in view of Ueda, as combined above, discloses the method of claim 8 above, wherein the first and third metal layers include molybdenum (Mo, Ueda, col. 17, lines 22-30).

As to claim 11, APA in view of Ueda, as combined above, discloses the method of claim 9 above, wherein the first and third metal layers are formed of the same material (Mo, Ueda, col. 17, lines 22-30).

As to claim 12, APA in view of Ueda, as combined above, discloses the method of claim 9 above.

The method of claim 9 above does not explicitly disclose a device wherein the first and third metal layers are formed of different materials.

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Ueda teaches the use of a refractory metal of Cr or a Mo-Ta alloy (col. 12, lines 62-67) as art recognized equivalents suitable for the intended purpose of forming an undercoat conductive layer (MPEP 2144.07).

Ueda is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to use Cr or a Mo-Ta alloy for one of the first or third metal layers, resulting in the claimed method wherein the first and third metal layers are formed of different materials.

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of APA in view of Ueda with the Cr or a Mo-Ta alloy for one of the first or third metal layers, resulting in the claimed method wherein the first and third metal layers are formed of different materials.

As to claim 13, APA in view of Ueda, as combined above, discloses the method of claim 9 above, wherein; the second metal layer includes aluminum (Al, Ueda, col. 17, lines 22-30).

As to claim 14, APA in view of Ueda, as combined above, discloses the method of claim 9 above, wherein the first and third metal layers include molybdenum (Mo, Ueda, col. 17, lines 22-30).

As to claim 15, APA in view of Ueda, as combined above, discloses the method of claim 8 above, wherein the patterning of the first metal layer and second semiconductor layer define channel region includes removing a portion of the first metal layer and second metal layer corresponding to the gate electrode and exposing the first semiconductor layer (Figure 15F, and col. 17, lines 14-67).

Response to Arguments

Applicant's arguments filed on 29 July 04 have been fully considered but they are not persuasive.

Applicant's ONLY arguments are as follows:

- (1) Applicant has not admitted prior art.
- (2) APA does not teach or suggest a first metal layer on the second semiconductor layer, the first metal layer patterned in the same pattern as the second semiconductor layer such that the first metal layer and second semiconductor layer define the separation region.
- (3) APA does not teach or suggest patterning the first metal layer and the second semiconductor layer in a same pattern to be lined up and abut.

Examiner's responses to Applicant's ONLY arguments are as follows:

- (1) It is respectfully pointed out that MPEP 608.01(c) (2) clearly indicates that the content of the Background of the Invention section is to provide a description of the

related art that describes to the extent practical the state of the prior art or other information disclosed. Where applicable, the problems involved in the prior art or other information disclosed which are solved by the Applicant's invention should be indicated. Applicant's own reference in the Background of the Invention to Figures as being of a "conventional" device (Specification Pages 1-5) with Figures 1-5 "conventional" are consistent with requirement of MPEP 608.01(c) (2) to disclose such prior art, and the drawing labels should so reflect per MPEP 608.02(g). Please see also MPEP 707.05(b) which states that MPEP 609 sets forth the positive guidelines for Applicants, their Attorneys and Agents who desire to submit prior art for consideration by the U.S. Patent and Trademark Office. It is respectfully pointed out that Applicant's argument that "conventional" art is not "prior" art is not persuasive and possibly improper in view of the Ueda.

(2) It is respectfully pointed out that APA discloses in the specification, page 1, line 15, through page 5, line 24, (Figures 1-5) the method of manufacturing a liquid crystal display device comprising a first metal layer on the second semiconductor layer, the first metal layer patterned in the same pattern as the second semiconductor layer such that the first metal layer and second semiconductor layer define the channel, 30 (Applicant's separation region) per Figure 3C (specification page 3, lines 28-31). Please note that this is well known in the art to take only one photolithography pattern (Applicant's patterned in the same pattern).

(3) It is respectfully pointed out that APA discloses in the specification, page 1, line 15, through page 5, line 24, (Figures 1-5) the method of manufacturing a liquid

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crystal display device comprising patterning the first metal layer and the second semiconductor layer in a same pattern to be lined up and abut per Figure 3C (specification page 3, lines 28-31). Please note that this is well known in the art to take only one photolithography pattern (Applicant's patterned in the same pattern).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy L Rude whose telephone number is (571) 272-2301. The examiner can normally be reached on Monday through Thursday.

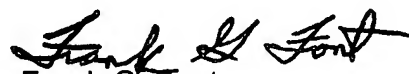
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



tlr

Timothy L Rude
Examiner
Art Unit 2883



Frank G. Font
Supervisory Patent Examiner
Technology Center 2800